IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

Abstract of the Disclosure

Structures and methods for in service programmable logic arrays with low tunnel barrier interpoly insulators are provided. The in-service programmable logic array includes a first logic and a second logic plan having a number of logic cells arranged in rows and columns that are interconnected to produce a number of logical outputs such that the in service programmable logic array implements a logical function. The logic cell includes a first source/drain region and a second source/drain region separated by a channel region in a substrate. A floating gate opposing the channel region and is separated therefrom by a gate oxide. A control gate opposes the floating gate. The control gate is separated from the floating gate by a low tunnel barrier intergate insulator. The low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5 and/or a Perovskite oxide tunnel barrier.